Module | Period | Assignments
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1 | Day 1 to Day 6 | 1. Write a program to evaluate the arithmetic statement:
X=(A-B + C * (D * E-F))/G + H*K
   a. Using a general register computer with three address instructions.
   b. Using a general register computer with two address instructions.
   c. Using an accumulator type computer with one address instructions.
   d. Using a stack organized computer with zero-address operation instructions.

2. A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

3. A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+ 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is
   a. direct
   b. indirect
   c. relative
   d. indexed

4. A relative mode branch type of instruction is stored in memory at an address equivalent to decimal decimal 750. The branch is made to an address equivalent to 500.
   a. What should be the value of the relative address field of the instruction (in decimal)?
   b. Determine the relative address value in binary using 12 bits. Why must the number be in 2's complement?)
   c. Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (b) is equal to the binary value of 500.

5. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R 1 contains the number 200. Evaluate the effective address
if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.

6. Let the address stored in the program counter be designated by the symbol X1. The instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) PC relative; (d) indexed?

7. An address field in an instruction contains decimal value 14. Where is the corresponding operand located for
   a. immediate addressing?
   b. direct addressing?
   c. indirect addressing?
   d. register addressing?
   e. register indirect addressing?

8. A PC-relative mode branch instruction is 3 bytes long. The address of the instruction, in decimal, is 256028. Determine the branch target address if the signed displacement in the instruction is –31.

9. A PC-relative mode branch instruction is stored in memory at address 620 10. The branch is made to location 530 10. The address field in the instruction is 10 bits long. What is the binary value in the instruction?

2 Day 7 to Day 19

1. The r’s complement of an n-digit number N in base r is defined as (r^n) - N for N! = 0 and 0 for N = 0. Find the tens complement of the decimal number 13250.

2. Assume numbers are represented in 8-bit twos complement representation. Show the calculation of the following:
   a. 6 + 13
   b. -6 + 13
   c. 6 - 13
   d. -6 – 13

3. Given x = 0101 and y = 1010 in twos complement notation (i.e., x = 5, y = -6), compute the product p = x * y with Booth’s algorithm.
4. Prove that the multiplication of two n-digit numbers in base B gives a product of no more than 2n digits.

5. Under computer integer arithmetic, the quotient J/K of two integers J and K is less than or equal to the usual quotient. True or false?

6. Express the following numbers in IEEE 32-bit floating-point format:
   a. -5
   b. -6
   c. -1.5
   d. 384
   e. 1/16
   f. -1/32

7. Consider a reduced 7-bit IEEE floating-point format, with 3 bits for the exponent and 3 bits for the significand. List all 127 values.

8. What would be the bias value for
   a. A base-2 exponent (B = 2) in a 6-bit field?
   b. A base-8 exponent (B = 8) in a 7-bit field?

9. Numerical values A and B are stored in the computer as approximations A' and B'. Neglecting any further truncation or roundoff errors, show that the relative error of the product is approximately the sum of the relative errors in the factors.

10. Perform the arithmetic operations ( +70) + ( +80) and ( -70) + ( -80) with binary numbers in signed-2’s complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal.

11. A 36-bit floating-point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero?

12. Show that the logic expression c n ⊕ c n−1 is a correct indicator of overflow in the addition of 2’s-complement integers by using an appropriate truth table.
13. An integer arithmetic unit that can perform addition and multiplication of 16-bit unsigned numbers is to be used to multiply two 32-bit unsigned numbers. All operands, intermediate results, and final results are held in 16-bit registers labeled R 0 through R 15 . The hardware multiplier multiplies the contents of R i (multiplicand) by R j (multiplier) and stores the double-length 32-bit product in registers R j and R j+1 , with the low-order half in R j . When j = i − 1, the product overwrites both operands. The hardware adder adds the contents of R i and R j and puts the result in R j . The input carry to an Add operation is 0, and the input carry to an Add-with-carry operation is the contents of a carry flag C. The output carry from the adder is always stored in C. Specify the steps of a procedure for multiplying two 32-bit operands in registers R 1 , R 0 , and R 3 , R 2 , high-order halves first, leaving the 64-bit product in registers R 15 , R 14 , R 13 , and R 12 . Any of the registers R 11 through R 4 may be used for intermediate values, if necessary. Each step in the procedure can be a multiplication, or an addition, or a register transfer operation.

14. Convert the decimal fraction 0.1 to a binary fraction. If the conversion is not exact, give the binary fraction approximation to 8 bits after the binary point using each of the three truncation methods.

3. Day 20 to Day 30

1. A 4-way set-associative cache memory unit with a capacity of 16KB is built using a block size of 8 words. The word length is 32-bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is

2. A RAM chip has a capacity of 1024 words of 8-bits each (1K x 8). The number of 2 x 4 decoders with enable line needed to construct a 16K x 16 RAM from 1K x 8 RAM is
(a) 4 (b) 5 (c) 6 (d) 7

3. a. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
   b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
   c. How many lines must be decoded for chip select? Specify the size of the decoders.

4. A computer uses RAM chips of 1024 x 1 capacity.
   a. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?
   b. How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.
A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bit in the tag field of an address is

(a) 11
(b) 14
(c) 16
(d) 27

6.

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit, respectively.

When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

7.

Consider a machine with a byte addressable main memory of $2^{16}$ bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50x50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that data cache is initially empty. The complete array is associated twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data cache misses will occur in total?
2. A user program could check for a zero divisor immediately preceding each division operation, and then take appropriate action without invoking the OS. Give reasons why this may or may not be preferable to allowing an exception interrupt to occur on an actual divide by zero situation in a user program.

3. Write a program that displays the contents of ten bytes of the main memory in hexadecimal format on a line of a display device. The ten bytes start at location LOC in the memory, and there are two hex characters per byte. The contents of successive bytes should be separated by a space when displayed.

4. Give an example of a RISC I instructions that operations.
   a. Decrement a register
   b. Complement a register
   c. Negate a register
   d. Clear a register to 0
   e. Divide a signed number by 4
   f. No operation

5. Write the RISC I instructions in assembly language that will cause a jump to address 3200 if the Z (zero) status bit is equal to 1.
   a. Using immediate mode
   b. Using a relative address mode (assume that PC = 340)

6. How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits.)
   a. Synchronous serial transmission.
   b. Asynchronous serial transmission with two stop bits.
   c. Asynchronous serial transmission with one stop bit.

7. A system uses a control memory of 1024 words of 32 bits each. The microinstruction has three fields. The microoperations field has 16 bits.
   a. How many bits are there in the branch address field and the select field?
   b. If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bit?
c. How many bits are left to select an input for the multiplexers?

8. The control memory has 4096 words of 24 bits each.
   a. How many bits are there in the control address register?
   b. How many bits are there in each of the four inputs shown going into the multiplexers?
   c. What are the number of inputs in each multiplexer and how many multiplexers are needed?

9. Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words.

10. Show how a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 microoperations. How many microoperations can be specified in one microinstruction?

11. A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
   a. Formulate a control word for a microoperation.
   b. Specify the number of bits in each field of the control word and give a general encoding scheme.
   c. Show the bits of the control word that specify the micro operation R4 = R5 + R6.